PCIe Gen4x4 M.2 2280 NVMe PS5033-E33 YMTC_EMS Data Sheet A0

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Revision History

Version	Description	Date	Remark
A0	Initial release	2025/8/25	

Contents

General Specification

Feature	Description
Capacity	512GB/1TB/2TB
Form Factor	M.2 2280(M Key)
PCIe Interface	NVME PCIe Gen 4 x 4 Lane
Compliance	PCI Express base 4.0/NVME 2.0
Performance	Sequential Read: 512GB up to 6752MB/s, 1TB up to 7094MB/s, 2TB up to 7049MB/s Sequential Write: 512GB up to 3308MB/s, 1TB up to 6456MB/s, 2TB up to 6464MB/s
IOPS (4K)	Random Read: 512GB up to 642K iops, 1TB up to 738K iops, 2TB up to 778K iops Random Write: 512GB up to 755K iops, 1TB up to 1124K iops, 2TB up to 1272K iops
Reliability	Mean Time Between Failure (MTBF): 1.5Million Hours Support global wear-leveling, bad block management algorithm Uncorrectable Bit Error Rate (UBER)<1 sector per 10^{16} bits read 512GB up to 340TBW 1TB up to 680TBW 2TB up to 1360TBW
Power Management	PCIE Active State Power Management (ASPM), 3.3V NVME Autonomous Power State Transition(ASPT), Support L1.2
Power Consumption	Idle < 1020mW (AVG) Active Write <3.98W (MAX) Active Read<4.50W (MAX)
Temperature	Operation : 0℃~70℃ Storage : -40℃~85℃
Humidity[2]	0% to 93%, non-condensing
Feature Support	Drive log Support HMB (Host Memory Buffer) LDPC ECC Protection
Vibration	10HZ~2000HZ / 16 GRMS
Shock	1500G @ 0.5 ms, Half-sine.
Weight	MAX 8g
Dimension(Max)	80.00±0.15mm x 22.00±0.15mm x 2.15±0.08mm(LxWxH)

Figures

Tables

1. Introduction

1.1. Description

QUANXING M.2 NVME SSD is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology in a small form factor for using a SSD and supporting Peripheral Component Interconnect Express (PCIe) 4.0 interface standard up to 4 lanes shows much faster performance than previous SSD. QUANXING M.2 NVME provide more performance in terms of bandwidth and lower latency than SAS and SATA based counterparts.

Part Number	Form Factor	Capacity
QXS3C512GPCYE000	M.2_2280	512GB
QXS3C001TPCYE000	M.2_2280	1TB
QXS3C002TPCYE000	M.2_2280	2TB

Table 1: Part Number

1.2 Functional Block Diagram

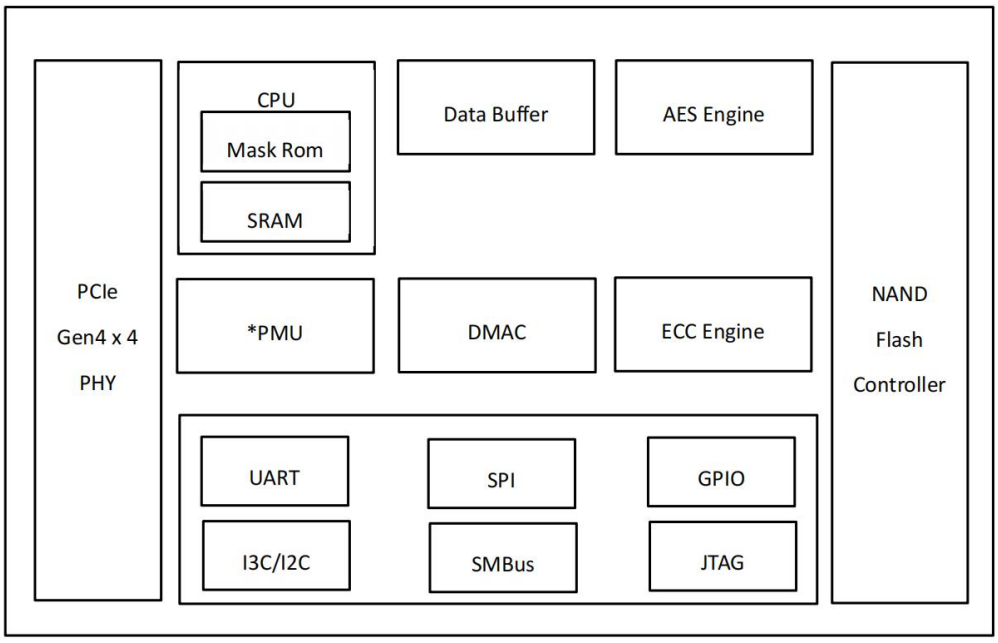


Figure 1-1 System Block Diagram

Figure 1: Functional Block Diagram

2. Product Specification

2.1Form Factor

M.2 Type 2280 Form Factor

2.2 Capacity

M.2 2280 : 512GB/1TB/2TB

Capacity	Available Density
512GB	476. 94GB
1TB	953.87GB
2TB	1907.73GB

Table 2: User Area

Notes:

- Nominal Capacity: 1 Gigabyte (GB) =1,000,000,000 bytes
- Unformatted Capacity: 1 Gigabyte (GB) =1,073,741,824 bytes
- IDEMA standard.
- Actual usable capacity may be less (due to formatting, partitioning, operating system, applications or otherwise)

3. Performance

Capacity	Sequential Read	Sequential Write	Random Read (4KB)	Random Write (4KB)
512GB	6752MB/s	3309MB/s	642K iops	755K iops
1TB	7094MB/s	6456MB/s	738K iops	1124K iops
2TB	7049 MB/s	6464 MB/s	778K iops	1272K iops

Table 3: Read and Write Performance

Notes:
- Actual performance may vary depending on use conditions and environment.
- Performance measured using CDM v8.0.4c/Random performance measured using AS SSD v 2.0.7.316 on Windows 10 64 bit.
- Sequential performance measured using 1MB data size. (QD=8 by Thrd 1).
- Random performance measured using 4 KB data size. (QD=1 by Thrd 64)

3.1 Ready Time

Type	Ready Time
Power on to Ready	Dependent on System HW and SW

Table 4: Specifications

Notes:

- Write cache enabled
- Device measured using Drive Master
- PCIe link speed is Gen 4x4.
- Test results may be different on different platform.
- Power on to ready time assumes proper shutdown (Power removal preceded by host Shutdown Notification)

3.2 Power Consumption

Parameter		Specification
Supply Voltage	Allowable Voltage	3.3V+/-5%
	Allowable noise/ripple	1~1MHZ, 120mVp-p

Table 5: Operating Voltage

Capacity	Product Status (w)		
	IDLE	Read	Write
512GB	990mW	3.71W	2.86W
1TB	990mW	3.98W	4.34W
2TB	1020mW	3.94W	4.50W

Table 6: Power Consumption

Notes:

- Data taken at 2
- Active maximum power is measured using HD Tune with overa sequentialwrite.
- NVME Low Power States supported.
- Actual power consumption may varies with ambient temperature, host platform and software settings.

3.3 Temperature

Environment	Mode	Min	Max	Unit
Ambient Temperature	Operating	0	70	℃
	Non-Operating	-40	85	℃
Humidity	Operating	0	90	%
	Non-Operating	0	93	%

Table 7: Temperature Relative Specifications

Note: Measured without condensation.

3.4 Reliability

Parameter	Value
Mean Time Between Failure (MTBF)	1,500,000 hours
Support global wear-leveling, bad block management algorithm	
Uncorrectable Bit Error Rate (UBER)	< 1 sector per 10^{16} bits read
Power On/Off Cycles	1,000 Times
Endurance	512GB : 340TBW 1TB : 680TBW 2TB : 1360TBW
Shock (Non-operating)	1500G @ 0.5ms, Half-sine
Vibration (Non-operating)	16 Grms/10~2KHZ

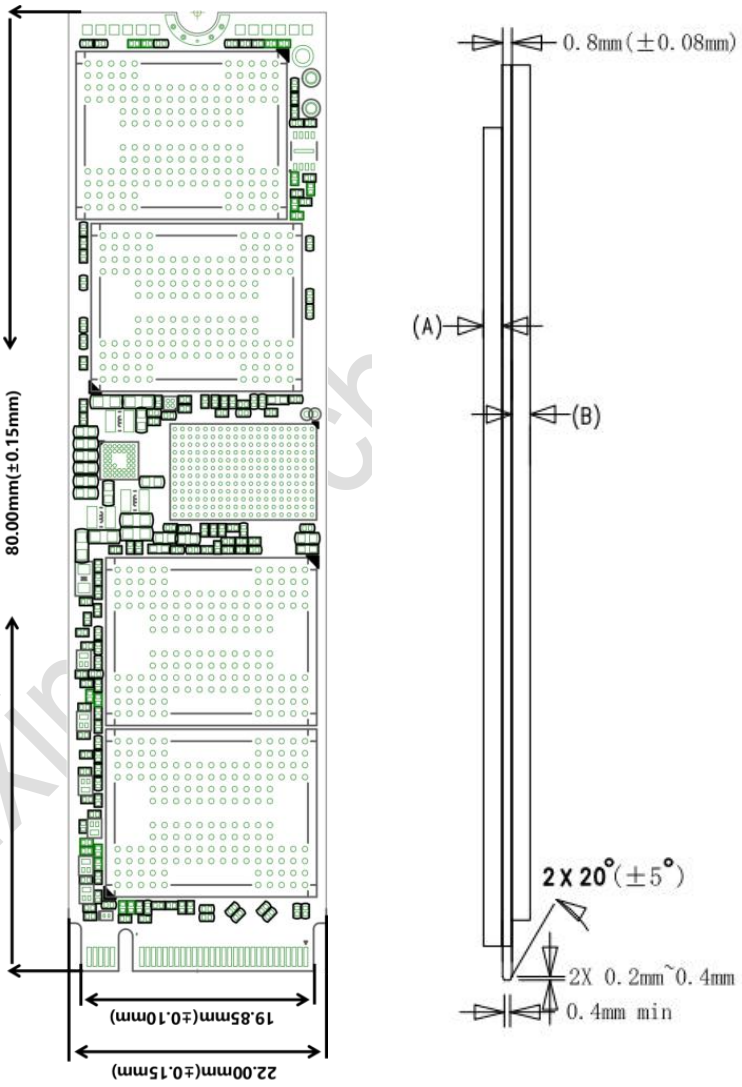
Table 8: Reliability Specifications

Note:

- MTBF is calculated based on a Part Stress Analysis. It assumes nominal voltage with all other parameters within specified range.
- Power on/off cycles is defined as power being removed from the drive, and the restored. Most host systems remove power from the drive when entering suspend and hibernate as well as on a system shutdown.Testing was conducted under Windows 11.
- Shock specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis.
- Vibration specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis. The measured specification is in root mean squared form

3.5 M.2 2280 SSD physical dimensions and Weight

Capacity	Height (mm)	Length (mm)	Width (mm)	Weight (gram)
512GB	2.15±0.08	80.00±0.15	22.00±0.15	MAX 8g
1TB	2.15±0.08	80.00±0.15	22.00±0.15	MAX 8g
2TB	2.15±0.08	80.00±0.15	22.00±0.15	MAX 8g



L	A(MAX)	B(MAX)
80.00mm	1.35mm	0

Figure 2: Mechanical Drawing

4. Pin Locations and Signal Descriptions

4.1 Pin Assignment and Description

The pin locations of the PCIe NVME SSD Gen 4 x 4 lane are shown below.

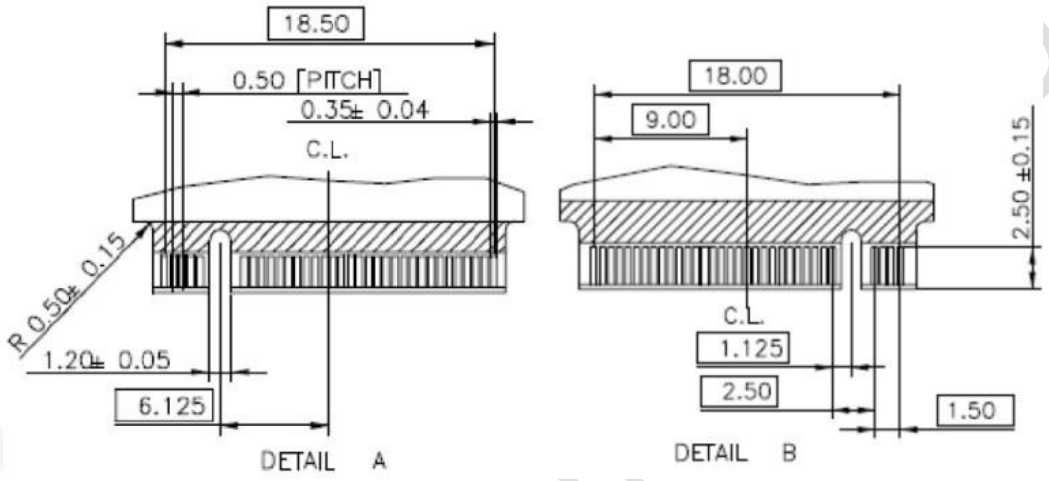


Figure 3: Pin Locations

Table 11 defines the signal assignment of the internal M.2 connector for SSD usage, described in the PCI Express M.2 specification version 1.0 of the PCI-SIG.

Pin No.	PCIe Pin	Description
1	GND	Return current path.
2	3.3V	PWR_1 source
3	GND	Return current path.
4	3.3V	PWR_1 source
5	PETn3	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
6*1	PWRDIS (I)(0/1.8/3.3V)	Active high with weak pull-down on Adapters. Power Disable notifies the Adapter to disable the power on the Adapter.
7	PETp3	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
8*1	PLN# (I)(0/1.8/3.3V)	Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the

		signal is asserted then it must ready itself for power loss.
9	GND	Return current path.
10*1	LED_1# (O)(OD)	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.
11	PERn3	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
12	3.3V	PWR_1 source
13	PERp3	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
14	3.3V	PWR_1 source
15	GND	Return current path.
16	3.3V	PWR_1 source
17	PETn2	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
18	3.3V	PWR_1 source
19	PETp2	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
20	NC	No connect
21	GND	Return current path.
22	VIO 1.8V	I/O source (low current)
23	PERn2	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
24	NC	No connect
25	PERp2	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
26*1	NC	No connect
27	GND	Return current path.
28*1	NC	No connect
29	PETn1	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
30*1	PLA_S3# (O)(0/1.8/3.3V)	Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.

31	PETp1	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
32	GND	Return current path.
33	GND	Return current path.
34	NC	No connect
35	PERn1	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
36	NC	No connect
37	PERp1	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
38	GND	Return current path.
39	GND	Return current path.
40*1	SMB_CLK (I/O)(0/1.8V)	SMBus clock. Open Drain with pull up on Platform
41	PETn0	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
42*1	SMB_DATA (I/O)(0/1.8V)	SMBus data. Open Drain with pull up on Platform
43	PETp0	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
44*1	ALERT#(O) (0/1.8V)	Alert notification to initiator. Open Drain with pull up on Platform. Active Low
45	GND	Return current path.
46	NC	No connect
47	PERn0	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
48	NC	No connect
49	PERp0	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
50	PERST# (I)(0/1.8V/3.3V)	PCIe Reset is a functional reset to the card as defined by the PCI Express BaseSpecification.
51	GND	Return current path.
52	CLKREQ#(I/O)(0/1.8V/3.3V)	PCIe Clock Request is a reference clock request signal as defined by the PCI Express Base Specification, also used by L1 PM Substates. Open Drain with pull up on Platform. Active Low.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express Base Specification.
54	NC	No connect
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express Base Specification.

56	Reserved for MFG_DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left NC in Platform Socket.
57	GND	Return current path.
58	Reserved for MFG_CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left NC in Platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67*1	NC	No connect
68	NC	No connect
69	PEDET = NC (PCIe)	Host interface Indication; to be grounded for SATA. No Connect for PCIe.
70	3.3V	PWR_1 source
71	GND	Return current path.
72	3.3V	PWR_1 source
73	VIO_CFG (O)	Sideband IO voltage indication. Signal with a weak pull-up on Platforms that support this function. When the Adapter supports 3.3V on the sideband IO signals, it must be connected to ground on the Adapter, otherwise it must be left unconnected on the Adapter. VIO_CFG of SSD device is default supports 3.3V on the sideband IO signals.
74	3.3V	PWR_1 source
75	GND	Return current path.

NOTES:

*1: Option Pins

5. Supported Command

5.1 Command List

Table 10: Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Commit
11h	Firmware Image Download
14h	Device Self-test

Table 11: Admin Commands-NVM Command Set Sepcific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

Opcode	Command Description
00h	Flush
01h	Write
02h	Read

04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management
0Ch	Verify

Table 12: NVM Commands

5.2 Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 13: Identify Controller Data Structure

Bytes	O/M	Description	Default Value
Controller Capabilities and Features			
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	SN
63:24	M	Model Number (MN)	Model Number
71:64	M	Firmware Revision (FR)	FW Name
72	M	Recommended Arbitration Burst (RAB)	0x6
75:73	M	IEEE OUI Identifier (IEEE)	Assigned by IEEE/RAC
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x06
79:78	M	Controller ID (CNTLID)	0x0000
83:80	M	Version (VER)	0x10400
87:84	M	RTD3 Resume Latency (RTD3R)	0x0007A120
91:88	M	RTD3 Entry Latency (RTD3E)	0x4C4B40

95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000200
99:96	M	Controller Attributes (CTRATT)	0x00000002
101:100	O	Read Recovery Levels Supported (RRLS)	0x0
109:102	-	Reserved	0x00
110	O	Power Loss Signaling Information	0x0
111	M	Controller Type (CNTRLTYPE)	0x01
127:112	O	FRU Globally Unique Identifier (FGUID)	0x00
129:128	O	Command Retry Delay Time 1 (CRDT1)	0x0000
131:130	O	Command Retry Delay Time 2 (CRDT2)	0x0000
133:132	O	Command Retry Delay Time 3 (CRDT3)	0x0000
239:134	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x00
Admin Command Set Attributes & Optional Controller Capabilities			
257:256	M	Optional Admin Command Support (OACS)	0x0017
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x07
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x1E
262	M	Error Log Page Entries (ELPE)	0xFF
263	M	Number of Power States Support (NPSS)	0x04
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01

267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x164
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x166
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0032
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00004000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00004000
295:280	O	Total NVM Capacity (TNVMCAP)	0x00
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0x00
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00000000
317:316	O	Extended Device Self-test Time (EDSTT)	0x000A
318	O	Device Self-test Options (DSTO)	0x01
319	M	Firmware Update Granularity (FWUG)	0x04
321:320	M	Keep Alive Support (KAS)	0x0000
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x0001
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x0111
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x0164
331:328	O	Sanitize Capabilities (SANICAP)	0xA0000002
335:332	O	Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS)	0x00000400
337:336	O	Host Memory Maximum Descriptors Entries (HMMAXD)	0x0010
339:338	O	NVM Set Identifier Maximum (NSETIDMAX)	0x0000
341:340	O	Endurance Group Identifier Maximum (ENDGIDMAX)	0x0000
342	O	ANA Transition Time (ANATT)	0x00
343	O	Asymmetric Namespace Access Capabilities (ANACAP)	0x00
347:344	O	ANA Group Identifier Maximum (ANAGRPMAX)	0x00000000

351:348	O	Number of ANA Group Identifiers (NANAGRPID)	0x00000000
355:352	O	Persistent Event Log Size (PELS)	0x00000060
511:356	-	Reserved	0x00
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x100
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0x56
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x00
525	M	Volatile Write Cache (VWC)	0x07
527:526	M	Atomic Write Unit Normal (AWUN)	0x00FF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x0000
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Namespace Write Protection Capabilities (NWPC)	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
543:540	O	Maximum Number of Allowed Namespaces (MNAN)	0x00000000
767:544	-	Reserved	0x00
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	non-zero
1791:1024	-	Reserved	0x00

2047:1792	-	Refer to the NVMe over Fabrics specification.	0x00
Power State Descriptors			
2079:2048	M	Power State 0 Descriptor (PSD0)	Bit[15:00]: 0x258
2111:2080	O	Power State 1 Descriptor (PSD1)	Bit[124:120]: 0x01 Bit[116:112]: 0x01 Bit[108:104]: 0x01 Bit[100:96]: 0x01 Bit[15:00]: 0x12C
2143:2112	O	Power State 2 Descriptor (PSD2)	Bit[124:120]: 0x02 Bit[116:112]: 0x02 Bit[108:104]: 0x02 Bit[100:96]: 0x02 Bit[15:00]: 0x96
2175:2144	O	Power State 3 Descriptor (PSD3)	Bit[124:120]: 0x03 Bit[116:112]: 0x03 Bit[108:104]: 0x03 Bit[100:96]: 0x03 Bit[95:64]: 0xDAC Bit[63:32]: 0x5DC Bit[25]: 0x1 Bit[24]: 0x1 Bit[15:00]: 0x1F4

2207:2176	O	Power State 4 Descriptor (PSD4)	Bit[124:120]: 0x04 Bit[116:112]: 0x04 Bit[108:104]: 0x04 Bit[100:96]: 0x04 Bit[95:64]: 0xAFC8 Bit[63:32]: 0x1388 Bit[25]: 0x1 Bit[24]: 0x1 Bit[15:0]: 0x32
……	O	(N/A)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00
Vendor Specific			
3081:3072	-	Reserved	0x00
3082	-	PLN feature options	0x00
3083	-	PLN feature options	0x00
4095:3084	-	Reserved	0x00

5.3 S.M.A.R.T Attributes

Table 16: SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[6]	1	Endurance Group Critical Warning Summary
[31:7]	25	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1
[215:202]	14	Reserved
[219:216]	4	Thermal Management Temperature Sensor 1 Transition Count
[223:220]	4	Thermal Management Temperature Sensor 2 Transition Count
[227:224]	4	Total Time For Thermal Management Temperature 1
[231:228]	4	Total Time For Thermal Management Temperature 2
[511:232]	280	Reserved