PCIE Gen3x4 M.2 2280 NVME

Data Sheet A0

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Revision History

Version	Description	Date	Remark
A0	Initial release	2025/06/05	

Contents

General Specification

Feature	Description
Capacity	128GB/256GB/512GB/1TB
Form Factor	M.2 2280(M Key)
PCIe Interface	NVME PCIe Gen 3 x 4 Lane
Compliance	PCI Express base 3.1/NVME 1.3
Performance	Sequential Read:128GB up to 1240MB/s,256GB up to 2450MB/s 512GB up to 2445MB/s,1TB up to 2565MB/s Sequential Write:128GB up to 1100MB/s,256GB up to 1835MB/s 512GB up to 1860MB/s,1TB up to 1890MB/s
IOPS (4K)	Random Read:128GB up to 48.5K iops,256GB up to 95.3K iops 512GB up to 178K iops,1TB up to 224K iops Random Write:128GB up to 202K iops,256GB up to 268K iops 512GB up to 270K iops,1TB up to 271K iops
Reliability	Mean Time Between Failure (MTBF): 1.5Million Hours Support global wear-leveling, bad block management algorithm Uncorrectable Bit Error Rate (UBER)<1 sector per 10^{16} bits read 128GB up to 85TBW,256GB up to 170TBW 512GB up to 340TBW,1TB up to 680TBW
Power Management	PCIE Active State Power Management (ASPM), 3.3V NVME Autonomous Power State Transition(ASPT), Support L1.2
Power Consumption	Idle < 500mW (AVG) Active Write <4W (MAX) Active Read<3.5W (MAX)
Temperature	Operation : 0℃~70℃ Storage : -40℃~85℃
Humidity[2]	5% to 95%, non-condensing
Feature Support	Power loss data protection for data-at-rest S.M.A.R.T/TRIM
Vibration	10HZ~2000HZ / 16 GRMS
Shock	1500G @ 0.5 ms, Half-sine.
Weight	< 10g
Dimension	80.00±0.2 mm x 22.00±0.2 mm x 2.15±0.15 mm (L x W x H)

Figures

Tables

1. Introduction

1.1. Description

QUANXING M.2 NVME SSD is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology in a small form factor for using a SSD and supporting Peripheral Component Interconnect Express (PCIe) 3.0 interface standard up to 4 lanes shows much faster performance than previous SSD. QUANXING M.2 NVME provide more performance in terms of bandwidth and lower latency than SAS and SATA based counterparts.

Part Number	Form Factor	Capacity
QXS2C128GN300000	M.2_2280	128GB
QXS2C256GN300000	M.2_2280	256GB
QXS2C512GN300000	M.2_2280	512GB
QXS2C001TN300000	M.2_2280	1TB

Table 1: Part Number

1.2 Functional Block Diagram

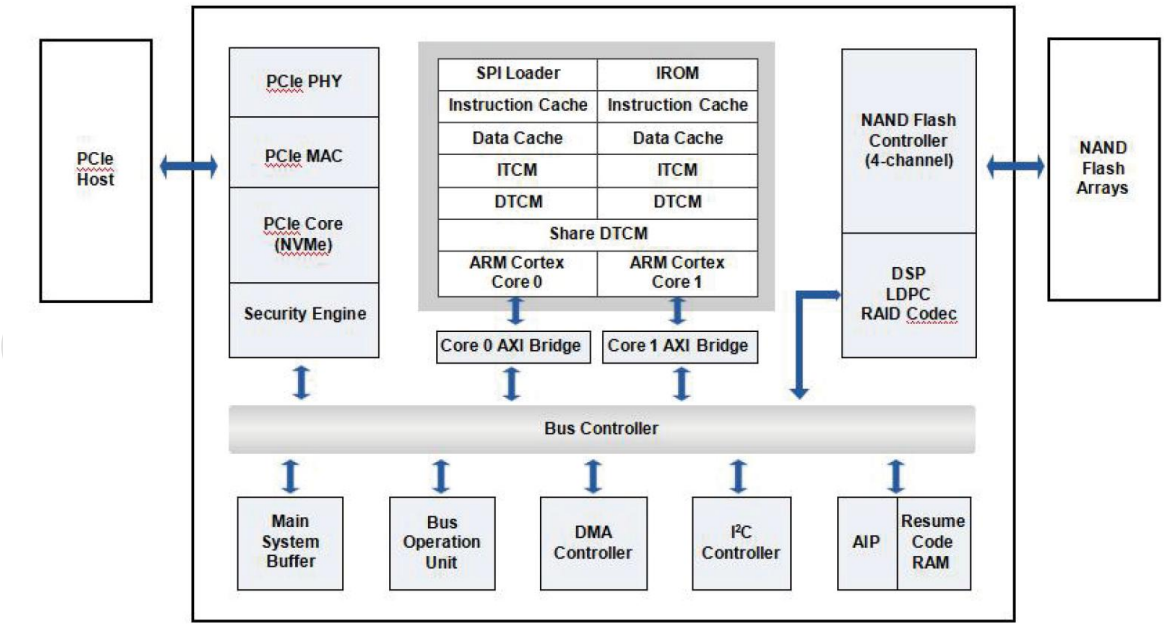

Figure 1: Functional Block Diagram

2. Product Specification

2.1Form Factor

M.2 Type 2280 Form Factor

2.2 Capacity

M.2 2280 : 128GB/256GB/512GB/1TB

Capacity	Available Density
128GB	119.24GB
256GB	238.47GB
512GB	476.94GB
1TB	953.87GB

Table 2: User Area

Notes:

- Nominal Capacity: 1 Gigabyte (GB) =1,000,000,000 bytes
- Unformatted Capacity: 1 Gigabyte (GB) =1,073,741,824 bytes
- IDEMA standard.
- Actual usable capacity may be less (due to formatting, partitioning, operating system, applications or otherwise)

3. Performance

Capacity	Sequential Read	Sequential Write	Random Read (4KB)	Random Write (4KB)
128GB	1240MB/s	1100MB/s	48.5K iops	202K iops
256GB	2450MB/s	1835MB/s	95.3K iops	268K iops
512GB	2445MB/s	1860MB/s	178K iops	270K iops
1TB	2565MB/s	1890MB/s	224K iops	271K iops

Table 3: Read and Write Performance

Notes:
- Actual performance may vary depending on use conditions and environment.
- Performance measured using CDM v8.0.4/Random performance measured using AS SSD v 2.0.7.316 on Windows 10 64 bit.
- Sequential performance measured using 1MB data size. (QD=8 by Thrd 1).
- Random performance measured using 4 KB data size. (QD=1 by Thrd 64)

3.1 Ready Time

Type	Ready Time
Power on to Ready	Dependent on System HW and SW

Table 4: Specifications

Notes:

- Write cache enabled
- Device measured using Drive Master
- PCIe link speed is Gen 3x4.
- Test results may be different on different platform.
- Power on to ready time assumes proper shutdown (Power removal preceded by host Shutdown Notification)

3.2 Power Consumption

Parameter		Specification
Supply Voltage	Allowable Voltage	3.3V+/-5%
	Allowable noise/ripple	1~1MHZ, 120mVp-p

Table 5: Operating Voltage

Capacity	Product Status (w)		
	IDLE	Read	Write
128GB	500mW	2.1W	2.1W
256GB	500mW	3W	3.1W
512GB	500mW	3.1W	3.3W
1TB	500mW	3.1W	3.8W

Table 6: Power Consumption

Notes:

- Data taken at 2
- Active maximum power is measured using Iometer with 128 KB sequentialwrite.
- NVME Low Power States supported.
- Actual power consumption may varies with ambient temperature, host platform and software settings.

3.3 Temperature

Environment	Mode	Min	Max	Unit
Ambient Temperature	Operating	0	70	℃
	Non-Operating	-40	85	℃
Humidity	Operating	5	95	%
	Non-Operating	5	95	%

Table 7: Temperature Relative Specifications

Note: Measured without condensation.

3.4 Reliability

Parameter	Value
Mean Time Between Failure (MTBF)	1,500,000 hours
Support global wear-leveling, bad block management algorithm	
Uncorrectable Bit Error Rate (UBER)	< 1 sector per 10^{16} bits read
Power On/Off Cycles	1,000 Times
Endurance	128GB : 85TBW,256GB : 170TBW 512GB : 340TBW,1TB : 680TBW
Shock (Non-operating)	1500G @ 0.5ms, Half-sine
Vibration (Non-operating)	16 Grms/10~2KHZ

Table 8: Reliability Specifications

Note:

- MTBF is calculated based on a Part Stress Analysis. It assumes nominal voltage with all other parameters within specified range.
- Power on/off cycles is defined as power being removed from the drive, and the restored. Most host systems remove power from the drive when entering suspend and hibernate as well as on a system shutdown.
- Shock specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis.
- Vibration specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis. The measured specification is in root mean squared form.

3.5 Weight

Weight : 10g (max)

3.6 Mechanical Drawing

Size: 80.00±0.2mm * 22.00±0.2mm * 2.20±0.15mm (L x W x H)

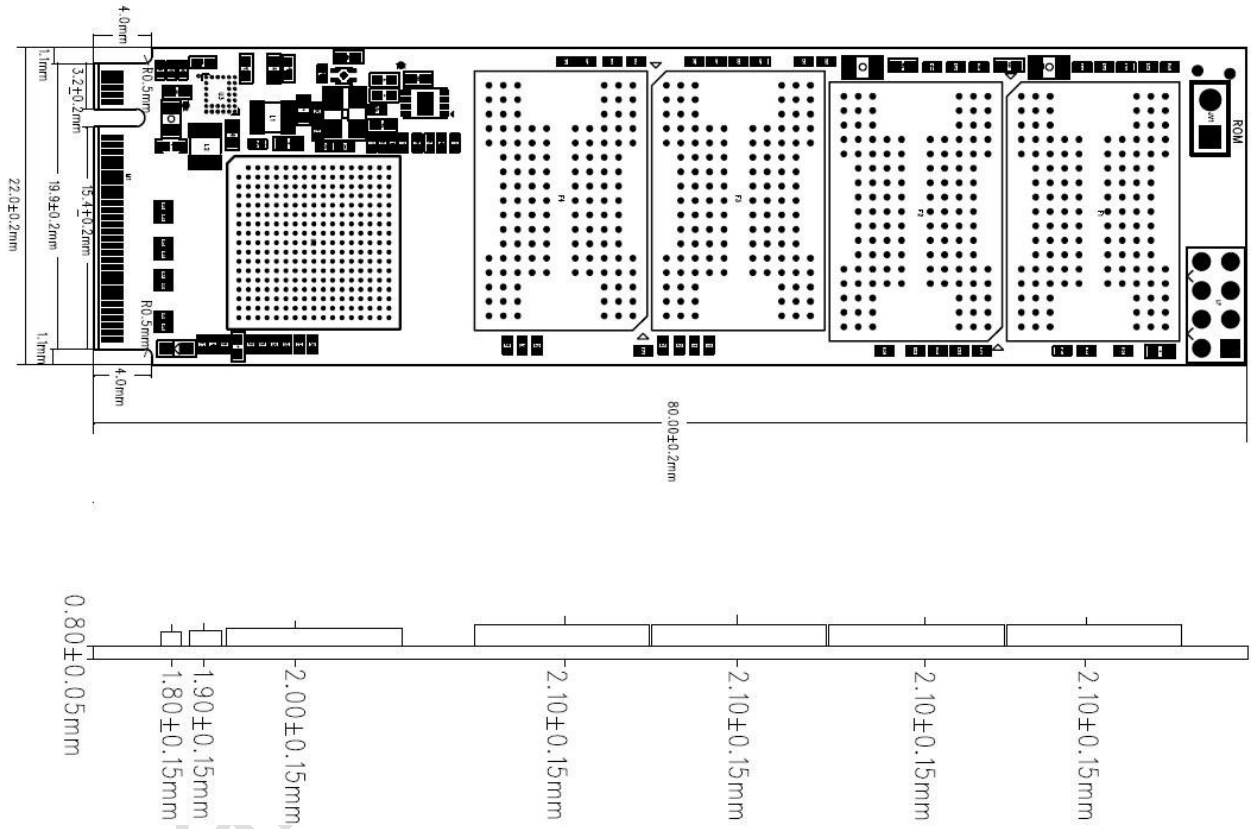

Figure 2: Mechanical Drawing

4. Pin Locations and Signal Descriptions

4.1 Pin Assignment and Description

The pin locations of the PCIe NVME SSD Gen 3 x 4 lane are shown below.

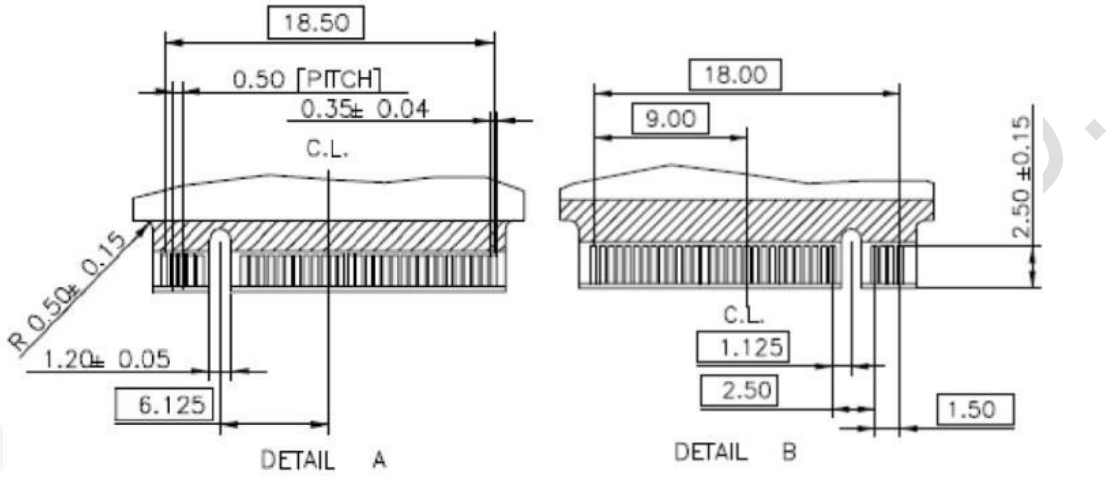

Figure 3: Pin Locations

Table 9: defines the signal assignment of the internal M.2 connector for SSD usage, described in the PCI Express M.2 specification version 1.0 of the PCI-SIG.

1	GND	Return Current Path	2	+3.3V	3.3V Power (Source)
3	GND	Return Current Path	4	+3.3V	3.3V Power (Source)
5	PETn3	PCIe TX	6	N/A	Reserved
7	PETP3	PCIe TX	8	N/A	Reserved
9	GND	Return Current Path	10	LED1#	Device Activity Signal
11	PERn3	PCIe RX	12	+3.3V	3.3V Power (Source)
13	PERp3	PCIe RX	14	+3.3V	3.3V Power (Source)
15	GND	Return Current Path	16	+3.3V	3.3V Power (Source)
17	PETn2	PCIe TX	18	+3.3V	3.3V Power (Source)
19	PETp2	PCIe TX	20	N/A	Reserved
21	GND	Return Current Path	22	N/A	Reserved
23	PERn2	PCIe RX	24	N/A	Reserved
25	PERp2	PCIe RX	26	N/A	Reserved
27	GND	Return Current Path	28	N/A	Reserved
29	PETn1	PCIe TX	30	N/A	Reserved
31	PETp1	PCIe TX	32	N/A	Reserved
33	GND	Return Current Path	34	N/A	Reserved
35	PERn1	PCIe RX	36	N/A	Reserved
37	PETp1	PCIe RX	38	N/A	Reserved
39	GND	Return Current Path	40	N/A	Reserved
41	PETn0	PCIe TX	42	N/A	Reserved
43	PERP1	PCIe TX	44	N/A	Reserved
45	GND	Return Current Path	46	N/A	Reserved
47	PERn0	PCIe RX	48	N/A	Reserved
49	PERp0	PCIe RX	50	PERST#	PCIe Reset

51	GND	Return Current Path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	Reserved
55	REFCLKP	PCIe Reference Clock	56	N/A	Reserved
57	GND	Return Current Path	58	N/A	Reserved
59	Notch	M Key	60	Notch	M Key
61	Notch	M Key	62	Notch	M Key
63	Notch	M Key	64	Notch	M Key
65	Notch	M Key	66	Notch	M Key
67	N/A	Removed	68	SUSCLK	Reserved
69	PEDET	Removed	70	+3.3V	3.3V Power (Source)
71	GND	Return Current Path	72	+3.3V	3.3V Power (Source)
73	GND	Return Current Path	74	+3.3V	3.3V Power (Source)
75	GND	Return Current Path			

5. Supported Command

5.1 Command List

Table 10: Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event

	Request
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test

Table 11: Admin Commands-NVM Command Set Sepcific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

Table 12: NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

5.2 Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 13: Identify Controller Data Structure

Description	Bytes	O/M	Default Value
PCI Vendor ID	01:00	M	tbd
PCI Subsystem Vendor ID	03:02	M	tbd
Serial Number (ASCII), #:Variables	23:04	M	tbd
Model Number (ASCII)	63:24:00	M	(see PN table)
Firmware Revision, #:Variables	71:64	M	tbd
Recommended Arbitration Burst	72	M	tbd
IEEE OUI	75:73	M	tbd

Controller Multi-Path I/O and Namespace Sharing Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function 0h - Controller is associated with a PCI Function. Bit 1: 1h - Device has Two or More controller 0h - Device has One Controller Bit 0: 1h- Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port	76	O	tbd
Maximum Data Transfer Size Bit 0: 1h - Supported (dual port – future value) 0h - Not Support (Single Port) Maximum Data Transfer Size (MDTS)	77	M	tbd

Description	Bytes	O/M	Default Value
Controller ID (CNTLID)	79:78	M	tbd
Reserved	255:80	M	tbd
Optional Admin Command Support Bits 15:3 - Reserved Bit 3: 1h - Namespace Management and Namespace Attachment Commands Supported (PM953 conditionally supports the Namespace Management and Namespace Attachment command(NVMe v1.2 specification) for reconfigurable overprovisioning) Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0 Security Send and Security Receive Not Supported	257:256	M	tbd
Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)	258	M	tbd
Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)	259	M	tbd
Firmware Updates Bits 7:4 – Reserved Bits 3:1 –Number of firmware slots Bit 0 – 1h Slot 1 is read only	260	M	tbd
Log Page Attributes Bits 7:1 – Reserved Bit 0: 0h SMART data is global for all namespaces	261	M	tbd
Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)	262	M	tbd
Number of Power States Support (0's based value)	263	M	tbd
Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in NVM Express 1.0c Figure 8	264	M	tbd
Autonomous Power State Transition Attributes (APSTA)	265	O	tbd
Reserved	511:266	-	-
Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)	512	M	tbd
Completion Queue Entry Size Bits 7:4 – 4h Max SQES (16 bytes) Bits 3:0 – 4h Required SQES (16 bytes)	513	M	tbd
Reserved	515:514	-	tbd

Number of Namespaces	519:516	M	tbd
Optional NVM Command Support Bits 15:6 – Reserved Bit 5 – 1h Reservations Supported 0h Not support Reservations Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 1h Write Uncorrectable Supported 0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare	521:520	M	tbd
Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported	523:522	M	tbd

Description	Bytes	O/M	Default Value
Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase Bit 1 – 1h Secure Erase Per Namespace Bit 0 – 0h Format Per Namespace	524	M	tbd
Volatile Write Cache 0h – No VWC present	525	M	tbd
Atomic Write Unit Normal	527:526	M	tbd
Atomic Write Unit Power Fail (0's based value)	529:528	M	tbd
NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express 1.1.a	530	M	tbd
Reserved	531	M	tbd
ACWU	533:532	O	tbd
Reserved	534:533	M	tbd
No SGL support	539:536	O	tbd
Reserved	703:540	-	tbd
Reserved	2047:704	-	tbd
Power State 0 Descriptor	2079:2048	M	refer to 'Identify Power State Descriptor Data Structure'
N/A	2111:2080	O	tbd
N/A	2143:2112	O	tbd
N/A	-	-	tbd

Power State 31 Descriptor (N/A)	3071:3040	0	tbd
Reserved	4095:3072	1	-

Table 14: Identify Namespace Data Structure & NVM Command Set Specific.

Bytes	Description
7:0	Namespace Size (NSZE)
15:8	Namespace Capacity (NCAP)
23:16	Namespace Utilization (NUSE)
24	Namespace Features (NSFEAT)
25	Number of LBA Formats (NLBAF)
26	Formatted LBA Size (FLBAS)
27	Metadata Capabilities (MC)
28	End-to-end Data Protection Capabilities (DPC)
29	End-to-end Data Protection Type Settings (DPS)
30	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	Reservation Capabilities (RESCAP)
119:32	Reserved
127:120	IEEE Extended Unique Identifier (EUI64)
131:128	LBA Format 0 Support (LBAF0)
135:132	LBA Format 1 Support (LBAF1)
139:136	LBA Format 2 Support (LBAF2)
143:140	LBA Format 3 Support (LBAF3)
147:144	LBA Format 4 Support (LBAF4)
151:148	LBA Format 5 Support (LBAF5)
155:152	LBA Format 6 Support (LBAF6)
159:156	LBA Format 7 Support (LBAF7)
163:160	LBA Format 8 Support (LBAF8)
167:164	LBA Format 9 Support (LBAF9)
171:168	LBA Format 10 Support (LBAF10)
175:172	LBA Format 11 Support (LBAF11)
179:176	LBA Format 12 Support (LBAF12)
183:180	LBA Format 13 Support (LBAF13)

187:184	LBA Format 14 Support (LBAF14)
191:188	LBA Format 15 Support (LBAF15)
383:192	Reserved
4095:384	Vendor Specific (VS)

5.3 S.M.A.R.T Attributes

Table 16: SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1
[203:202]	2	Temperature Sensor 2
[205:204]	2	Temperature Sensor 3
[207:206]	2	Temperature Sensor 4